Dolphin Technology

WHAT DOLPHIN CUSTOMERS ARE SAYING

"THE BEST RAM TECHNOLOGY"

As VP of IC Engineering at Tilera Corporation and a customer of TSMC, I am submitting this testimonial for Dolphin Technology, an IP provider for TSMC. Tilera Corporation has used Dolphin Technology RAMs, ROMs, and I/Os across the 90nm, 40nm and 28nm nodes.

Tilera benchmarks consistently show that Dolphin has the best RAM technology, beating other top vendors in all dimensions – frequency, area and power. Dolphin's I/O IP incorporated important features starting in 90nm and below, technologies that other leading vendors have yet to implement in 28nm.

Dolphin understands that Tilera is a small company and provides flexibility and early access to technology. They support Tilera during design and well past first silicon, helping debug our issues, accepting feedback, and continuing to tune and improve their offerings. For example, Dolphin kept Tilera informed and updated as they tuned IP to accommodate the 6σ process variations seen in recent technologies. Dolphin fully embraces making their customers successful.

Dolphin has continued to expand their IP offerings to include extensive standard cell libraries, DfT tools and protocol controllers. The growth is planned and pertinent. Recently, they have instituted a customer tracking system that is increasing the quality of release mechanisms and product collateral.

Dolphin Technology has been an excellent partner for 8+ years.

John F. Brown III
Vice President, IC Engineering
Tilera Corporation

"A TRUSTED SUPPLIER AND PARTNER"

Since 2007, Sigma Designs has utilized Dolphin Technology's products in multiple projects across multiple process nodes. This includes Dolphin IP such as SRAM Memory Compilers (Single Port, Dual Port, 1-Port and 2-Port), Via ROM Memory Instances, Standard Cell Libraries (both High Density and High Speed) and DDR PHY Interfaces.

The first process node where Sigma used Dolphin IP was 90GP, and we have since used it in 55GP and 40LP as well. Dolphin has repeatedly met our highest expectations about the quality of both the IP and the ongoing support we receive, and they have firmly established themselves as a trusted supplier and partner.

Jacques Martinella
Vice President, Engineering
Sigma Designs

"THE BEST DENSITY AND SPEED AT MINIMUM POWER"

We at GEO have used Dolphin Technology's IP in several products, and each time, we have been very pleased with the results.

In particular, we have found Dolphin's SRAM Compilers to provide the best density and speed at minimum power. Their Standard Cell and I/O Libraries are also highly competitive in density, features, power and speed.

Sudhir Chandratreya
Vice President, Engineering
GEO Semiconductor

"USED IN MULTIPLE PROJECTS ACROSS MULTIPLE PROCESS NODES"

Juniper Networks has utilized Dolphin Technology's SRAM and standard cell products in multiple projects across multiple process nodes.

Dolphin has repeatedly met our expectations about the quality of both the IP and the ongoing support we receive, and over the years, they have established themselves as a trusted supplier and partner.

Bharat Bisen
Senior Director of Engineering
Juniper Networks

Front End views are available under NDA. For more information, contact: sales@dolphin-ic.com

Dolphin Technology, Inc. 333 W Santa Clara Street, Suite 920 San Jose, CA 95113
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MEMORY COMPILERS I/O STANDARD CELLS

All IP's also available for 5nm/5nm+, 6nm, 7nm/7nm+, 12nm and 22nm

STANDARD MEMORY & SPECIALTY MEMORY	16nm FF+ FFC	28nm HP, HPx LP, ULP	40nm G, LP ULP	55nm GP, LP ULP, EF	65nm GP LP	80nm G GC	90nm G, GT EF
Single-Port & Dual-Port SRAM Compiler - Ultra Low Power / Ultra Low Leakage (RAMpiler®)	●[1]	●[1]	●[1]	●[1]	●[1]	●[1]	●[1]
Single-Port & Dual-Port SRAM Compiler - High Performance and High Density (RAMpiler®)	●[1]	●[1]	●[1]	●[1]	●[1]	●[1]	●[1]
Pseudo Dual-Port SRAM Compiler - Higher Performance, Higher Density, Lower Power (RAMpiler®)	●[1]	●[1]					
1-Port & 2-Port Register File Compiler - High Density and High Performance (RAMpiler®)	●	●	●	●	●	2-Port (1R/1W)	2-Port (1R/1W)
Binary BCAM and Ternary TCAM Compiler (CAMpiler®)	●	●	●	●	●	●	●
Via Programmable ROM and Diffusion ROM Compiler	●	●	●	●	●	●	●
Custom Register Files (4R/1W, 4R/2W, 3R/3W, 8R/1W, etc.)	●[R]	●[R]	●[R]	●[R]	●[R]	●	●[R]
Memory Test & Repair (BIST)	●	●	●	●	●	●	●

GENERAL PURPOSE I/O & SPECIALTY I/O							
General Purpose I/O (GPIO)	●	●	●	●	●	●	●
I2C Interface	●	●	●	●	●	●	●
PVT compensated drive strength buffer	●	●	●	●	●	●	●
PLL Compiler	●	●	●	●	●	●	●
HSTL/SSTL Class I/II/III (DDR Combo)	●	●	●	●	●	●	●
DDR4/3/2 & LPDDR3/2 PHY Interface	●	●					
DDR/3/2 & LPDDR2/1 PHY Interface			●	●	●	●	●
DLL for High Performance and Low Power products (digital)	67-1067 MHz	67-1067 MHz	67-1067 MHz	200-800 MHz	200-800 MHz		
LVPECL	●[R]	●[R]			●	●	●
LVDS drivers and receivers	●[R]	●	●[R]	●	●	●	●
LVDS/LVPECL combo pad	●[R]	●[R]	●[R]	●[R]	●[R]	●	●
Multi-Function I/O Interface (LVDS, DDR4/3/2, HSTL/SSTL, LVTTL/LVCMOS, PCI 66/PCIX-133)	●[R]	●[R]	●[R]	●	●	●	
PCI-X 133 MHz and PCI-66/33 MHz	●[R]	●[R]	●[R]	●[R]	●[R]	●	●
PCI-Express	●[R]	●[R]	●[R]	●[R]			
HyperTransport® (HT-PHY)	●[R]	●[R]	●[R]	●[R]	●[R]	●	●[R]
Fibre Channel PHY, XAUI Ethernet Interface	●[R]	●[R]	●[R]	●[R]	●[R]	●[R]	●[R]
SPI4.2 with Dynamic De-skew	●[R]	●[R]	●[R]	●[R]	●[R]		
SerDes with up to 10G CDR (SATA, SAS, etc.)	●[R]	●[R]	●[R]	●[R]			

STANDARD CELLS							
Ultra High Density 6-track	●	●[2]	●	●	●		
High Perf & High Density 7.5-track, Very HP 10.5-track	●						
Ultra Low Power & Ultra High Density 7-track		●	●	●	●	●	●
High Performance & Ultra High Density 9-track	●	●					
High Performance & High Density 10-track		●	●	●	●	●	●
Ultra High Performance & High Density 12-track	●	●	●				
Ultra High Performance 14-track		●					

[1] Without Redundancy [2] 6.5-track for 28HPC [R] Upon Request

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DDR PHY DDR CONTROLLER DDR PLL/DLL

DDR PHY	16nm FF+ FFC	28nm HP, HPx LP, ULP	40nm G, LP ULP	55nm GP, LP ULP, EF	65nm GP LP	80nm G GC	90nm G, GT EF
DDR4/3/2 PHY (DFI 3.1 compliant)	●	●	●				
LPDDR3/2 PHY (DFI 3.1 compliant)	●	●	●				
DDR3/2 PHY (DFI 3.1 compliant)			●	●	●		
Maximum speed, with 1.8V oxide (Mbps)	3200	3200	2133	1600	1600		
Maximum speed, with 2.5V oxide (Mbps)	1600	1600	1600	1600	1600		
IP is split into two hard macros (one for commands, control and address pins, one for 8-bit data bus)	●	●	●	●	●		
Supports custom number of address bits	●	●	●	●	●		
Compensation controller and pads for automatic driver and receiver termination impedance calibration	●	●	●	●	●		
Slew rate control, per-bit de-skew, gate training, read and write leveling	●	●	●	●	●		
JTAG signals for Mentor/Synopsys and LogicVision	●	●	●	●	●		
BIST with Pseudo Random Pattern Generator	●	●	●	●	●		
Scannable flops	●	●	●	●	●		
Wirebond, flip-chip and cup configurations	●	●	●	●	●		

DDR CONTROLLER							
DFI 3.1 Interface with Matching or 1:2 Frequency Ratio	●	●	●	●	●	●	●
Built-in Gate Training and Read/Write Leveling	●	●	●	●	●	●	●
Maximum speed (Mbps)	3200	3200	2133	1600	1600	1600	1600
JEDEC Standard DDR4/3/2 and LPDDR3/2 SDRAM	●	●	●				
JEDEC Standard DDR3/2 and LPDDR2 SDRAM				●	●	●	●
Multi-port configurable AXI4 interface w/QoS signaling	●	●	●	●	●	●	●
Multi-port arbitration engine with programmable dynamic priority algorithm	●	●	●	●	●	●	●
Pipeline option for frequency vs. latency tradeoff	●	●	●	●	●	●	●
Fully configurable for various performances and requirements	●	●	●	●	●	●	●
FPGA portable (Xilinx PHY & Altera PHY compatible)	●	●	●	●	●	●	●
BFM verification suite	●	●	●	●	●	●	●
Single AXI4-Lite programming interface	●	●	●	●	●	●	●
AXI4 dynamic QoS signaling for non-blocking communications	●	●	●	●	●	●	●
Support for low-latency bypass ports/channels	●	●	●	●	●	●	●
Advanced dynamic QoS support based on Queuing Theory and Traffic Hysteresis	●	●	●	●	●	●	●

DDR PLL / DLL							
PLL: Input Reference Clock 25MHz – 200MHz	●	●	●	●	●	●	●
PLL: Output Clock 200MHz – 2GHz	●	●	●	●	●	●	●
PLL: Divider Ratio 2 – 20	●	●	●	●	●	●	●
DLL: High Precision DLL	●	●	●	●	●	●	●
DLL: Coarse and fine controls to minimize resolution errors	●	●	●	●	●	●	●
DLL: External bypass and check of generated delay code	●	●	●	●	●	●	●

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eMMC/SD/SDIO I2C/I2S

eMMC/SD/SDIO – PHY & CONTROLLER	16nm FF+ FFC	28nm HP, HPx LP, ULP	40nm G, LP ULP	55nm GP, LP ULP, EF	65nm GP LP
Compliant with eMMC 5.1, SD 4.1 and SDIO 4.1 Specifications	●	●	●	●	●
Transfers data in HS400, HS200, DDR52, SDR52 compatibility modes	●	●	●	●	●
Supports HS400, HS200, DDR52 and SDR52 data transfer modes	●	●	●	●	●
Supports UHS-II (SD 4.0) data transfer rates up to 312MB/s	●	●	●	●	●
Supports UHS-I (SD 3.01) data transfer rates up to 104MB/s	●	●	●	●	●
Supports 32-bit and 64-bit system data bus and addressing	●	●	●	●	●
Tuning for HS200 mode	●	●	●	●	●
4KB block support	●	●	●	●	●
32 bit DMA interface	●	●	●	●	●
Interrupts and wake up functionality	●	●	●	●	●
Supports both Asynchronous and Synchronous AXI4 Interface	●	●	●	●	●
AXI4 Narrow Transfer	●	●	●	●	●
Enhanced strobe function for reliable operation at HS400 mode.	●	●	●	●	●
Host clock rate variable between 0 and 200 MHz	●	●	●	●	●
Transfers the data in 1-bit, 4-bit and 8-bit modes	●	●	●	●	●
Supports Low-Power mode	●	●	●	●	●
Supports CUP/Wirebond and Flip Chip configurations	●	●	●	●	●
Precision master/slave digital DLL is used for timing circuits.	●	●	●	●	●
PHY uses 6 metal layers. Higher metals are configurable for improved power and ground mesh	●	●	●	●	●
PHY includes built-in DLL (50-200 MHz) to handle high-speed operations	●	●	●	●	●
IDDQ Model	●	●	●	●	●
PVT compensation	●	●	●	●	●
Power supplies include Core VDD, I/O VDD and VSS	●	●	●	●	●
No use of deep n-well devices	●	●	●	●	●
Interrupts and wake up functionality	●	●	●	●	●

I2C/I2S - PHY & CONTROLLER					
Drive programmable	●	●	●	●	●
Multi-mode support	●	●	●	●	●
Built in JTAG support for Mentor/LogicVision models	●	●	●	●	●
NAND or XOR tree select	●	●	●	●	●
Int/Out Register option	●	●	●	●	●
Pull down and sustain option	●	●	●	●	●
1.8 oxide	●	●	●	●	●
Metastability removal	●	●	●	●	●
Noise filter	●	●	●	●	●
Bus Start/Stop, stuck low detection	●	●	●	●	●
Signals (SDA/SCL) generation with user-defined timing constraints	●	●	●	●	●
Clock (SCL) synchronization	●	●	●	●	●
Bus arbitration	●	●	●	●	●
Customized I2C I/O:	●	●	●	●	●
• 1.8V / 2.5V oxide	●	●	●	●	●
• Multi-mode support	●	●	●	●	●
• Full power bus strapping based on metallization/top metal requirements (horizontal and vertical metallization option available from M6 and above)	●	●	●	●	●
• Available in Wirebond, Flip Chip and CUP configurations	●	●	●	●	●

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DOLPHIN technology partners & CUSTOMERS

PARTNERS

Dolphin Technology maintains cooperative partnerships with numerous industry leaders, enhancing the breadth and quality of our products and services.

These relationships enable us to offer value-added services to our customers, such as:

- Providing early access to test chip development
- Understanding customer roadmap requirements
- Providing early demand visibility
- Reducing time to market

Electronic Design Automation (EDA) Partners:

- Cadence
- Legend Design Technology
- Magma Design Automation
- Mentor Graphics
- Synopsys

Design for Testability (DFT) Partners:

- LogicVision
- Mentor Graphics
- Syntest

Memory Controller Partners:

- Northwest Logic

CUSTOMERS

Since 1996, Dolphin has worked with over 100 customers and completed hundreds of design projects. Our extensive, fab-verified offerings have met the most rigorous standards of the industry's most demanding companies.

Here are just a few of the industry-leading companies that trust and rely on Dolphin products:

- Avago
- Broadcom
- Cisco Systems
- Ericsson
- eSilicon
- EZchip
- Geo Semiconductor
- HiSilicon
- IDT
- Intel
- Juniper Networks
- Lattice Semiconductor
- LSI
- MCST
- Microchip
- Novatek
- Onsemi
- Qualcomm
- Sigma Designs
- SRISA
- Texas Instruments
- Toshiba
- And many more

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